APPENDIX
"Clean Copy"

Page 1, line 6:

CROSS-REFERENCES TO RELATED APPLICATIONS

This application is a continuation of Application No. 08/754,337 filed November 22, 1996, which issued as U.S. Patent No. 5,794,003 on August 11, 1998; which is a continuation of Application No. 08/498,135 filed July 5, 1995, now abandoned; which is a continuation of Application No. 08/147,797 filed November 5, 1993, now abandoned; the disclosures of which are incorporated by reference for all purposes.

This application also incorporates by reference for all purposes Application No. 08/422,753 filed April 13, 1995, which issued as U.S. Patent No. 5,560,028 on September 24, 1996; which is a continuation of Application No. 08/147,800 filed November 5, 1993, now abandoned.

Paragraph beginning page 4, line 5:

Figure 1 is a block diagram of a computer system incorporating the associative crossbar switch according to the preferred embodiment of this invention. The following briefly describes the overall preferred system environment within which the crossbar is incorporated. For additional information about the system, see Application No. 08/422,753 filed April 13, 1995, which issued as U.S. Patent No. 5,560,028 on September 24, 1996; which is a continuation of Application No. 08/147,800 filed November 5, 1993, now abandoned, and entitled "Software Scheduled Superscaler Computer Architecture," which is incorporated by reference herein. FIG. 1 illustrates the organization of the integrated circuit chips by which the computing system is formed. As depicted, the system includes a first integrated circuit 10 that includes a central processing unit, a floating point unit, and an instruction cache.

Pending Claims:

131. A processor comprising:
a register file having a plurality of registers;
an instruction set including instructions which address the registers, each instruction being one of a plurality of instruction types;
a plurality of execution units, each execution unit being one of a plurality of types, wherein each instruction type is executed on one or more execution unit types;
and further wherein the instructions are encoded in bundles, each bundle including a plurality of instructions and a template field grouped together in a N-bit field, the instructions being located in instruction slots of the N-bit field, the template field specifying a mapping of the instruction slots to the execution unit types.

132. The processor of claim 131 wherein the template field further specifies instruction group boundaries within the bundle, with an instruction group comprising a set of statically contiguous instructions that are executed concurrently.